

UTILITY APPLICATION

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FOR

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ON

**LOW COST DIELECTRIC ISOLATION METHOD FOR INTEGRATION OF
VERTICAL POWER MOSFET AND LATERAL DRIVER DEVICES**

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**LOW COST DIELECTRIC ISOLATION METHOD FOR INTEGRATION OF
VERTICAL POWER MOSFET AND LATERAL DRIVER DEVICES**

Cross Reference to Related Patent Applications

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The present patent application is related to
copenpending U.S. Patent Application Serial No. 10/753,030,
filed January 6, 2004, Attorney Docket No. 112518.00007,
entitled "Selective Epi-Region Method for Integration of
Vertical Power MOSFET and Lateral Driver Devices" and
filed by Badredin Fatemizadeh et al.

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Field of the Invention

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[0001] The present invention relates in general to
semiconductor devices and, more particularly, to a
dielectric isolation method for integration of power
MOSFET and lateral driver device.

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Background of the Invention

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[0002] Metal oxide semiconductor field effect
transistors (MOSFETs) are commonly used in power
transistor applications such as switching power supplies,
power conversion, power management, energy systems,
telecommunications, personal computer applications, motor
control, automotive, and consumer electronics. Power
devices generally refer to transistors and other
semiconductor devices that are capable of switching about
1.0 ampere or more of conduction current. Power MOSFETs
are well known as high input impedance, voltage-
controlled devices which require a relatively small
charge to initiate turn-on from simple drive circuitry.

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The power MOSFET ideally exhibits high drain-to-source current carrying capacity, low drain-to-source resistance (R_{DSon}) to reduce conduction losses, high switching rate with low switching losses, and high safe operating range (SOA) which provides the ability to withstand a combination of high voltage and high current.

[0003] Power MOSFETs are often vertical devices used in combination with a lateral driver circuit. The driver circuit may be as simple as a p-channel transistor and an n-channel transistor connected in a totem-pole arrangement. Other driver circuits are known to have additional features. The junction between the drain of the p-channel transistor and the drain of the n-channel transistor is the output of the driver circuit, which is coupled to the gate of the power MOSFET. In one operating mode, the p-channel transistor of the driver circuit is turned on to source current directly into the gate of the power MOSFET. In another operating mode, the n-channel transistor of the driver circuit is turned on to sink current directly away from the gate of the power MOSFET. The driver circuit must supply sufficient current to charge and discharge the gate voltage of the power MOSFET. The driver circuit thus operates to turn on and off the power MOSFET in a rapid and efficient manner.

[0004] The driver circuit is typically a low voltage device, operating in the range of 5-25 volts. The power MOSFET is a higher voltage device, operating in the range of 20-30 volts. The lateral driver circuit is usually placed on the same base silicon substrate as the power device. For efficient layout considerations, the lateral driver circuit is often located in proximity to the power MOSFET.

[0005] In constructing the lateral devices, an N-epi layer is disposed above the silicon substrate. A first p-well is formed in the N-epi layer for the n-channel transistor, and an n-well is formed within the first p-well for the p-channel transistor. A second p-well is also formed in the N-epi layer for the power device. The second p-well is located in proximity to but separated from the first p-well by an N-epi region.

[0006] Depending on the operating voltage and operating frequency of the power device, the lateral driver circuit may be subject to junction leakage in the form of carrier injection from the power device. The lateral driver circuit can also be subjected to switching noise from power device. The first and second p-wells are separated by N-epi, which form a PN junction. The PN junction ideally provides isolation, but can become forward biased in certain circumstances. Any conduction between the power MOSFET and driver circuit could be problematic or detrimental to the operation of the IC.

[0007] A need exists to maintain isolation between the power MOSFET and the lateral driver circuit.

Summary of the Invention

[0008] In one embodiment, the present invention is a method of forming a semiconductor device comprising the steps of providing a substrate, forming a first layer of semiconductor material over the substrate, removing a portion of the first layer to provide a layer offset between a removed portion of the first layer and a remaining portion of the first layer, forming an oxide layer of uniform thickness over the removed portion of the first layer and the remaining portion of the first

layer, planarizing the oxide layer so that the oxide layer over the remaining portion of the first layer is removed, forming a polysilicon region over the planarized oxide layer, forming an epi region over the remaining
5 portion of the first layer, forming a trench between the polysilicon region and the epi region extending vertically down to the oxide layer, and depositing oxide in the trench down to the oxide layer to isolate the polysilicon region.

10 **[0009]** In another aspect, the present invention is a method of forming an integrated circuit having a driver device in proximity to a power device comprising the steps of forming an oxide layer below the driver device, forming a trench between the driver device and the power
15 device, wherein the trench extends down to the oxide layer, and depositing oxide in the trench down to the oxide layer to isolate the driver device from the power device.

20 **[00010]** In yet another aspect, the present invention is a semiconductor device having a driver device in proximity to a power device. The semiconductor device is made by the process comprising the steps of forming an oxide layer below the driver device, forming a trench between the driver device and the power device, wherein
25 the trench extends down to the oxide layer, and depositing oxide in the trench down to the oxide layer to isolate the driver device from the power device.

30 **[00011]** In yet another aspect, the present invention is a semiconductor device comprising a first semiconductor device. A second semiconductor device is physically proximate and electrically coupled to the first semiconductor device. An oxide layer is disposed below the first semiconductor device. An oxide-filled trench

is disposed between the first and second semiconductor devices. The oxide-filled trench extends down to the oxide layer to provide isolation between the first and second semiconductor devices.

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Brief Description of the Drawings

[00012] FIG. 1 is a schematic diagram of a driver circuit and power MOSFET;

10 FIGs. 2-7 illustrate cross-sectional views of a first embodiment of the driver circuit and power MOSFET device; and

FIGs. 8-12 illustrate cross-sectional views of a second embodiment of the driver circuit and power
15 MOSFET device.

Detailed Description of the Drawings

[00013] Referring to FIG. 1, driver circuit 10 is shown
20 with an output coupled to the gate of power MOSFET 12. Driver circuit 10 and power MOSFET 12 are formed in proximity to one another on a single silicon substrate and packaged as an integrated circuit (IC) 20. IC 20 may contain other signal processing circuitry. The IC
25 containing power MOSFET 12 is commonly used in power transistor applications such as switching power supplies, power conversion, power management, energy systems, telecommunications, personal computer applications, motor control, automotive, and consumer electronics.

30 [00014] Driver circuit 10 must supply sufficient current to charge and discharge the gate voltage of power MOSFET 12. Power MOSFET 12 is capable of switching more than 1.0 ampere of conduction current I_{12} . Power MOSFET

12 exhibits high drain-to-source current carrying capacity, low drain-to-source resistance (R_{DSon}) to reduce conduction losses, high switching rate with low switching losses, and high safe operating range (SOA) which provides the ability to withstand a combination of high voltage and high current.

[00015] Driver circuit 10 includes p-channel transistor 14 and n-channel transistor 16. A control signal is applied to the common gates of transistors 14 and 16. If the control signal is low, then transistor 14 conducts and transistor 16 is turned off. Transistor 14 sources current to the gate of power MOSFET 12 to turn on the power device in a rapid manner. If the control signal is high, then transistor 14 turns off and transistor 16 conducts. Transistor 16 sinks current away from the gate of power MOSFET 12 to turn off the power device in a rapid manner.

[00016] Driver circuit 10 operates with a low supply voltage V_{DD1} on the order of 5-25 volts and ground potential. Power MOSFET 12 operates with a higher supply voltage V_{DD2} in the range of 20-30 volts or more, and supply voltage V_{SS2} . As noted above, driver circuit 10 and power MOSFET 12 are formed in proximity to one another on the same silicon substrate within IC 20.

Depending on the operating voltage and operating frequency of power MOSFET 12, driver circuit 10 may be subjected to parasitic components and junction leakage in the form of carrier injection from the power device. The lateral driver circuit 10 can also be subjected to switching noise from power MOSFET 12. In general, the lateral devices of driver circuit 10 will require isolation and protection from the higher operating voltage of power MOSFET 12.

[00017] Turning to FIG. 2, a cross-sectional view of IC 20 is shown. Line A marks the boundary between the lateral driver device area, i.e., where driver circuit 10 is to be formed, and the vertical power device area, i.e., where power MOSFET 12 is to be formed. IC 20 includes silicon substrate 22 having an N+ doping concentration. Substrate 22 is doped with N-type semiconductor material such as phosphorus or arsenic at a concentration level of 1×10^{20} atoms/centimeter (cm)³.

Substrate 22 is about 200-250 microns in thickness. Substrate 22 provides structural support for IC 20 and forms the drain of the vertical power MOSFET 12. N+ layer 24 is disposed over substrate 22. N+ layer 24 has a thickness of about 2 microns and is doped with N-type semiconductor material on the order of 1×10^{19} phosphorus or arsenic atoms/cm³.

[00018] In one aspect, N+ layer 24 can be a separate semiconductor layer with respect to substrate 22. In another aspect, N+ layer 24 functions as an extension of, and can be considered an integral part of, substrate 22. In another embodiment, the area defined by substrate 22 and N+ layer 24 can be a single uniform-concentration substrate region. In another view, N+ layer 24 can be omitted altogether.

[00019] Mask layer 26 is disposed over a portion of N+ layer 24 corresponding to the vertical power device area, i.e., that area to the right of line A. The portion of N+ layer 24 corresponding to the lateral driver device area, i.e., that area to the left of line A, is unprotected in the subsequent etching process. With mask layer 26 in place, the portion of N+ layer 24, which is under the lateral driver device area, is etched away substantially down to substrate 22. Mask layer 26 is

then removed as shown in FIG. 3. After the etching process, there is a 2-micron offset or stair-step 28 between substrate 22 and N+ layer 24 at the boundary between the lateral driver device area and the vertical power MOSFET area.

[00020] The portion of N+ layer 24 that has been etched away constitutes the removed portion of N+ layer 24. The portion of N+ layer 24 that had been under mask layer 26 constitutes the remaining portion of N+ layer 24. The etching process may be stopped before reaching substrate 22, may be stopped at substrate 22, or may continue into substrate 22. The height of offset 28 is thus determined by the original thickness of N+ layer 24, and the degree or amount of etching that takes place, all of which can be controlled by the design and manufacturing process.

[00021] An oxide layer 30 having dielectric properties is grown or formed to a relatively uniform thickness of about 1-2 microns across substrate 22 and N+ layer 24. The thickness of oxide layer 30 above substrate 22 to the left of line A is approximately the same as the thickness of oxide layer 30 above N+ layer 24 to the right of line A. In the process of growing oxide layer 30, the offset or stair-step 28 between substrate 22 and N+ layer 24 causes a similar offset or stair-step 32 in oxide layer 30 as shown. The offset 32 may be a step function, gradual, angled, or inclined, with a linear or non-linear slope.

[00022] Oxide layer 30 is planarized in FIG. 4 with etch-back and polish steps to create a flat or even surface across the lateral driver device area and the vertical power device area, i.e., on both sides of line A. In the step of planarizing oxide layer 30, the oxide to the right of line A is completely removed. There is

no oxide in the vertical power device area to the right of line A because any oxide under power MOSFET 12 could adversely effect the operation of the vertical power device.

5 **[00023]** In FIG. 5, an N-type semiconductor region is grown or formed to a relatively uniform thickness of about 4-6 microns across oxide layer 30 and N+ layer 24. The N-type semiconductor region receives an N- doping concentration of phosphorus or arsenic on the order of
10 5×10^{15} to 5×10^{16} atoms/cm³. The N-type semiconductor region over oxide layer 30 becomes polysilicon region 36. The N-type semiconductor region over N+ layer 24 becomes epi layer 38.

15 **[00024]** Polysilicon region 36 undergoes re-crystallization process such as zone melting re-crystallization (ZMR) in which the polysilicon is annealed to melt the silicon. The polysilicon re-crystallizes as a single crystalline region.

Semiconductor devices formed in region 36 can be either
20 poly-crystalline or mono-crystalline. For example, thin film transistors (TFT) may be used for driver circuit 10 in both poly and mono-crystalline form.

25 **[00025]** In FIG. 6, mask layer 40 is disposed over the re-crystallized polysilicon region 36 and N-epi region 38 with an opening for trench 42. Trench 42 is formed around the lateral driver device area by an etching process which extends vertically down to oxide layer 30. In one embodiment, trench 42 overlaps line A. That is, trench 42 is formed in both the lateral driver device
30 area and vertical power device area to overlap oxide layer 30 and N+ layer 24. In another embodiment, trench 42 is formed entirely in the lateral driver device area, extending down to oxide layer 30. Trench 42 is filled

with oxide. The oxide-filled trench 42 is continuous with oxide layer 30. Accordingly, the combination of oxide layer 30 and oxide-filled trench 42 completely surrounds and provides dielectric isolation for the lateral driver device area from the electrical effects of power MOSFET 12. The oxide barrier provides isolation from parasitic components, carrier injection, and noise immunity for driver circuit 10. The dielectric isolation of oxide layer 30 and oxide-filled trench 42 also provides a thermal barrier against the heat generated by power MOSFET 12.

[00026] In FIG. 7, p-well 46 is implanted in polysilicon region 36 in the lateral driver device area for driver circuit 10. N-channel transistor 16 is formed in p-well 46. An N-well 50 is implanted in p-well 46 for p-channel transistor 14. P-well 46 has a doping concentration on the order of 1×10^{16} to 5×10^{17} boron atoms/cm³. A p-well 52 is implanted in N-epi region 38 in the vertical power device area for power MOSFET 12. P-well 52 has a doping concentration on the order of 1×10^{17} to 5×10^{17} boron atoms/cm³. A trench 56 is formed for the gate of power MOSFET 12 and source regions 58 are formed on both sides of trench 56. Substrate 22 is the drain of power MOSFET 12. When driver circuit 10 charges the gate of power MOSFET 12, a conduction path for current I_{12} is created from source regions 58, vertically along trench 56, to the drain in substrate 22. Although power MOSFET 12 is shown as a vertical device, the power MOSFET can be formed as a lateral device.

[00027] It can be seen in FIG. 7 that the combination of oxide layer 30 and oxide-filled trench 42 surrounds polysilicon region 36, p-well 46, and lateral driver circuit 10. The oxide barrier formed by oxide layer 30

and oxide-filled trench 42 provides dielectric isolation for transistors 14 and 16 in driver circuit 10 from the electrical effects of power MOSFET 12. The oxide barrier prevents carrier injection and parasitic components into the lateral driver device area and isolates switching noise and heat generated by power MOSFET 12.

[00028] An alternate embodiment of IC 20 is shown in FIGs. 8-12. Returning to FIG. 2 as a starting point, the alternate embodiment begins with silicon substrate 22 overlaid with N+ layer 24. Mask layer 26 is disposed over a portion of N+ layer 24 and a portion of N+ layer 24 corresponding to the lateral driver device area, i.e., that area to the left of line A, is etched away, substantially down to substrate 22.

[00029] In FIG. 8, mask layer 26 is removed and an epi layer 60 is formed to a relatively uniform thickness of about 6 microns across substrate 22 and N+ layer 24. The thickness of epi layer 60 above substrate 22 to the left of line A is approximately the same as the thickness of epi layer 60 above N+ layer 24 to the right of line A. In the process of forming N-epi layer 60, the offset or stair-step between substrate 22 and N+ layer 24 causes a similar offset or stair-step to N-epi layer 60, as shown.

[00030] N-epi layer 60 is planarized in FIG. 9 with etch-back and polish steps to create a flat or even surface across the lateral driver device area and the vertical power device area. A mask layer 62 is placed over the planar surface of N-epi layer 60 in order to form another offset or stair-step in N-epi layer 60 by etching away the area unprotected by mask layer 62.

[00031] The resulting offset or stair-step 64 in N-epi layer 60 is shown in FIG. 10. Mask layer 62 is removed and oxide layer 68 is grown or formed to a relatively

uniform thickness of about 1-2 microns across N-epi layer 60. The thickness of oxide layer 68 below the lateral driver device area is approximately the same as the thickness of oxide layer 68 below the vertical power device area. In the process of growing oxide layer 68, the offset or stair-step 64 causes a similar offset or stair-step 70 in oxide layer 68 as shown.

[00032] Oxide layer 68 is planarized in FIG. 11 with etch-back and polish steps to create a flat or even surface across the lateral driver device area and the vertical power device area. In the step of planarizing oxide layer 68, the oxide above the vertical power device area is completely removed. An N-type semiconductor region is formed to a relatively uniform thickness of about 4-6 microns across oxide layer 68 and N-epi layer 60. The N-type semiconductor region receives an N-doping concentration of phosphorus or arsenic on the order of 5×10^{15} to 5×10^{16} atoms/cm³. The N-type semiconductor region over oxide layer 68 becomes polysilicon region 74. The N-type semiconductor region over N-epi layer 60 becomes epi layer 76. Polysilicon region 74 undergoes re-crystallization process such as ZMR to re-crystallize the polysilicon as a single crystalline region.

[00033] Mask layer 78 is disposed on the re-crystallized polysilicon region 74 and N-epi region 76 with an opening for trench 80. Trench 80 is formed around the lateral driver device area by an etching process extending vertically down to oxide layer 68. Trench 80 is filled with oxide. The oxide-filled trench 80 is continuous with oxide layer 68. Accordingly, the combination of oxide layer 68 and oxide-filled trench 80 completely surrounds and isolates the lateral driver

device area from the electrical effects of power MOSFET 12. The oxide barrier provides isolation from carrier injection, parasitic components, and noise immunity for driver circuit 10. The dielectric isolation of oxide layer 68 and oxide-filled trench 80 also provides a thermal barrier against the heat generated by power MOSFET 12.

[00034] In FIG. 12, p-well 82 is implanted in polysilicon region 74 in the lateral driver device area for driver circuit 10. N-channel transistor 16 is formed in p-well 82. An N-well 84 is implanted in p-well 82 for p-channel transistor 14. A p-well 86 is implanted in N-epi region 76 in the vertical power device area for power MOSFET 12. A trench 90 is formed for the gate of power MOSFET 12 and source regions 92 are formed on both sides of trench 90. Substrate 22 is the drain of power MOSFET 12. When driver circuit 10 charges the gate of power MOSFET 12, a conduction path for current I_{12} is created from source regions 92, vertically along trench 90, to the drain in substrate 22.

[00035] The offset 70 in the oxide layer 68, corresponding to offset 64, which in turn is determined by the thickness of N⁺ layer 24 and the depth of the etching process, creates the portion of the oxide isolation barrier under the lateral driver device area. The height of the offset 70 controls the thickness of the oxide layer under the later driver device area. The width of trench 80 determines the thickness of the sidewalls of the oxide isolation barrier. The oxide barrier provides isolation for driver circuit 10 from the electrical effects of power MOSFET 12.

[00036] The above principals are equally applicable to providing isolation between transistors 14 and 16 in

driver circuit 10. An oxide-filled trench is formed around and between one or both of the transistors 14-16 extending down to the oxide layer 68 using process steps similar to those described above. The n-channel transistor would be dielectrically-isolated from the p-channel transistor. This would be particularly useful when implementing TFTs as the driver devices.

[00037] A person skilled in the art will recognize that changes can be made in form and detail, and equivalents may be substituted for elements of the invention without departing from the scope and spirit of the invention. The present description is therefore considered in all respects to be illustrative and not restrictive, the scope of the invention being determined by the following claims and their equivalents as supported by the above disclosure and drawings.